D. Remarks

No Grounds For Rejection Presented for Claim 21.

Applicant added new claim 21 in the responsive amendment submitted with the Request for Continued Examination, dated 8/25/2003. No grounds of rejection have been presented for this claim. Accordingly, the burden of prosecution cannot have been met for this claim.

Applicant notes that any rejection of this claim in a subsequent office action will be a new ground for rejection – and hence cannot be a final rejection.

Rejection of Claims 8, 9 and 12 Under 35 U.S.C. §103(a), based on U.S. Patent No. 4,679,304 (*Bois*) in view of Japanese Patent Publication 62-216268 (A) (*Goto*) and further in view of U.S. Patent No. 5,731,221 (*Kwon*).

The invention of claim 8 is directed to a manufacturing method of a semiconductor device. The method includes depositing a stacked film including a first conductive layer in contact with a first oxide film. The stacked film and first oxide film are etched to form a plurality of stacked film patterns.

The semiconductor substrate is oxidized to form a second oxide film on a surface of the semiconductor substrate sandwiched between stacked film patterns and a surface of the semiconductor substrate. The second oxide film is formed below end portions of the stacked film patterns. The second oxide film has a film thickness thicker than the first oxide film.

The method further includes forming a side wall mask film on a side of the stacked film patterns and removing the portion of the second oxide film sandwiched between the mask patterns to form a trench. The trench is filled with an insulating film. The stacked film includes a stopper film that provides a stopper for a chemical mechanical polishing step.

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

Applicant traverses this rejection based on a number of arguments and requests action as set forth in separate sections below.

1. Request for Translation of Foreign Language Reference to Establish Right of Petition Under 37 C.F.R. 1.181

The rejection has relied on *Goto*, which is entirely in the Japanese language apart from an Abstract. The obviousness rejection is based on various claims regarding *Goto*:

> One of ordinary skill in the art reviewing Bois would pursue use of the mask of Japan '268 because it is useful as a LOCOS mask which is the reasoning used in the rejections...[1]

Thus, the rejection states that there is some teaching in *Goto* that would indicate the mask shown by the reference is "useful as a LOCOS mask". It is not understood from where this reasoning is derived, as nothing in the Abstract indicates so. In any event, reliance on only selected portions of a foreign reference is not believed to be sufficient for proper examination:

> It is our opinion that a proper examination under 37 CFR § 1.104 should be based on the underlying document *and translations*, where needed. Accordingly, the preferred practice is for the examiner to cite and rely on the underlying document.[2]

> In the event a reference is in a foreign language... the applicant may wish to request the examiner supply a translation. If a translation is not supplied by the examiner, the applicant may wish to consider seeking supervisory relieve by way of petition (37 C.F.R. § 1.181) to have the examiner directed to obtain and supply a translation...[3]

Applicant requests that a translation of *Goto* be provided. It is believed that such a translation would enable the reference to be considered properly, as a whole. Further, it is believed that such a translation will bolster Applicant's case against combination with *Bois* by indicating in detail clear incompatibilities with the method of *Bois*.

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[1] See the Advisory Action, dated 7/25/03, first continuation sheet, Lines 5-6.
[2] In re Jones, 62 USPQ2d 1206, 1208 (B.P.A.I. 2001) (unpublished).
[3] In re Jones, 62 USPQ2d 1206, 1208-09 (B.P.A.I. 2001) (unpublished).

2. Prima Facie Case Not Established – All Claim Limitations Not Shown or Suggested

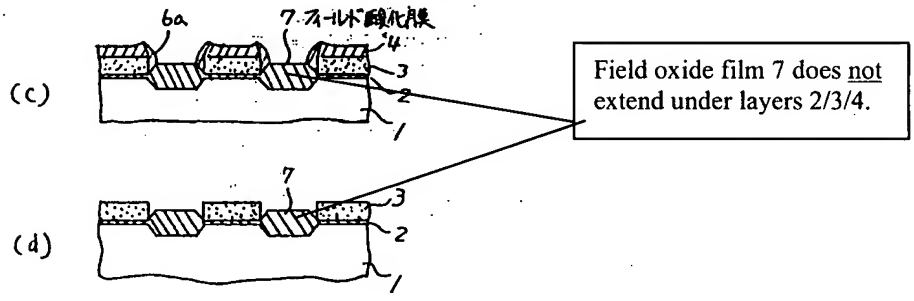
To arrive at Applicant's claim 8 limitations, the rejection appears to propose using a multiple films (first insulating film/conductive film/oxide film) of *Goto* as a mask shown in *Bois*.

> Japan '268 discloses LOCOS using a nitride 4/conductive film 3/oxide film 2. It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Japan '268 to enable the formation of the LOCOS mask of Bois.[4]

However, such an arrangement fails to arrive at Applicant's claim limitations.

Applicant's claim 8 recites a second oxide film that is thicker than the first oxide film. Further, such a second oxide film is below end portions of the stacked film patterns. Modifying *Bois* to employ the combination film of *Goto* results in a structure which does not show this limitation.

The combination film of *Goto*, when subjected to an oxidation step, produces an oxidized region (argued to correspond to Applicant's) that is not formed below the multiple films. This is evident in the figures of *Goto*:



As illustrated in the above figure, using the multiple layers of *Goto* in the process of *Bois* would not produce an oxidized film that extended under multiple layers. This is an intentional feature of *Goto* that teaches away from Applicant's claim limitations.

Goto seeks to form gate electrodes having a flattened surface:

[4] See the Office Action, dated 12/18/2003, Page 2, Last paragraph.

> The field oxide films are formed in self alignment manner to the gate electrode for the poly Si film 3... thereby the surface of the gate electrode can be flattened.[5]

Thus, it is undesirable for the field oxide film 7 of *Goto* to extend under such gate electrodes (which form part of the multiple layers), as this would result in gate electrodes that are not flat. Applicant believes the requested translation of the reference would clarify this point.

Thus, incorporating the multiple layers of *Goto* as a mask in the process of *Bois* would not result in an oxidized region that extends under such multiple layers. Therefore, the combination does not show or suggest all of Applicant's claim limitations, and a prima facie case of obviousness has not been established for this claim.

3. Prima Facie Case Rebutted– Reference Teaches Away From Invention.

As is well understood, a prima facie case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention.[6]

> [A] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.[7]

As understood from above, *Goto* leads in a direction away from the invention of claim 8, by emphasizing a field oxide film 7 that does not extend below the multiple layers 2/3/4 of *Goto* in order to achieve a flattened gate electrode film 3. This is in contrast to Applicant's invention which includes a second oxide film below end portions of a stacked film pattern.

Because one viewing *Goto* would be discouraged form pursuing the claimed invention, even if a prima facie case could be established, such a prima facie case would be rebutted. Again, a translation of *Goto* would clarify this issue.

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[5] See *Goto,* last sentence of the CONSTITUTION section.
[6] In re Geisler, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).
[7] In re Gurley, 31 USPQ 2d 1130, 1131 (Fed. Cir. 1994).

Dependent claim 12 includes additional limitations not shown in the cited reference.

Claim 12 recites that a second oxide film is 20-50 nm thicker than the first oxide film. Such a limitation would not be obvious as a matter of routine optimization, as Applicant's claim limitations fall well outside the general teachings of the references.

While the rejection is not clear about how specific claim elements correspond to features of the references, Applicant has assumed that the rejection is arguing that the isolating region 8 of *Bois* corresponds to Applicant's "second oxide film". *Bois* teaches that this region has a thickness of 300 nm. *Bois* provides no teachings regarding any layer corresponding to a first oxide film.

Applicant has also assumed that the rejection is arguing that gate oxide film 2 of *Goto* corresponds to Applicant's "first oxide film". The limited English language portion of *Goto* provides no value for the thickness of this gate oxide film 2.

Thus, because the cited combination of references provides no range value for a layer corresponding to Applicant's "first oxide film", no teachings regarding the conditions of claim 12 are shown (e.g., relative thicknesses between a first and second oxide).

Accordingly, Applicant's claim limitations cannot be a matter of routing optimization, as there is no value to optimize with respect to a first oxide layer.

For this reason, this ground for rejection is traversed.

Rejection of Claim 10 Under 35 U.S.C. §103(a), based on *Bois* in view of *Goto*, further in view *Kwon*, and further in view of U.S. Patent No. 5,106,772 (*Lai*)

To the extent that this ground of rejection relies on *Bois* in view of *Goto*, further in view *Kwon*, Applicant incorporates by reference herein the same general comments set forth above for claim 8.

Rejection of Claim 11 Under 35 U.S.C. §103(a), based on *Bois* in view of *Goto*, further in view *Kwon*, even further in view of U.S. Patent Application Publication US 2001/0011759 (*Rho et al.*) or U.S. Patent No. 5,693,542 (*Suh et al.*).

To the extent that this ground of rejection relies on *Bois* in view of *Goto*, further in view *Kwon*, Applicant incorporates by reference herein the comments set forth above for claim 8.

In addition, in rejecting claim 11 the Examiner admits that the combination does not show Applicant's claim 11 limitations, and takes official notice in order to establish a case for prima facie obviousness.

> The combination does not include forming the sidewalls using nitride. The examiner takes official notice that formation of nitride spacers as part of a hard mask was known prior to applicant's invention. It would have been within the scope of one of ordinary skill in the art to combine the know process with that of the combination to enable formation of the mask used to etch the LOCOS film.[8]

First, Applicant seasonably traverses this statement and requests the citation of references in support. Applicant notes that the arrangement of claim 12 cannot be read in a vacuum. The invention is not a simple utilization of a nitride spacer, but is the use of a nitride spacer in conjunction with the other limitations set forth in base claim 10. Thus, any reference in support of such official notice must address why one skilled in the art would employ such a spacer.

Second, this reasoning cannot establish a prima facie case of obviousness as it simply indicates that nitride spacers can be used, not why such use is desirable, advantageous, etc.

For these reasons, this ground for rejection is traversed.

Rejection of Claims 14 and 15 Under 35 U.S.C. §102(b) based on *Bois*.

Applicant's amended claim 14 invention is directed to a method that includes

a) forming a first oxide film on a surface of a semiconductor substrate;

b) depositing a stacked film different from the first oxide film and including a first layer on the first oxide film;

c) etching the stacked film and the first oxide film to form a plurality of stacked film patterns arranged on the semiconductor substrate;

d) oxidizing the semiconductor substrate to form a second oxide film on a surface of the semiconductor substrate sandwiched between adjacent stacked film patterns and a surface of the semiconductor substrate below end portions of the stacked film patterns wherein the second oxide film has a film thickness thicker than the first oxide film;

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[8] Office Action, dated 12/18/2003, Page 4, Lines 1-4.

e) removing the portion of the second oxide film sandwiched between the stacked film patterns and a portion of the underlying semiconductor substrate using the stacked film patterns as a mask to form a trench in the semiconductor substrate; and

f) filling the trench with an insulating film.

Thus, Applicant's amended claim 14 recites forming a first oxide film, and depositing a stacked film different from the first oxide film on the first oxide film. Such a limitation is not shown or suggested by *Bois*. *Bois* teaches the formation of isolation zones with a single mask layer.[9] Thus, if the mask layer corresponds to Applicant's first oxide film, the mask layer cannot be a different stacked film, and vice versa.

Accordingly, Applicant's amended claim 14 includes limitations not shown in the cited reference.

Amended dependent claim 15 also includes limitations not shown in the cited reference. Amended claim 15 recites that step of filling the trench with an insulating film includes forming the insulating film to have a top surface coplanar with the top surface of the first layer.

In *Bois*, a trench is filled with an isolating dielectric. However, such a dielectric is not coplanar with a top surface of the mask. [10]

Thus, amended claim 15 includes limitations not shown in the cited reference.

For all of these reasons, this ground for rejection is traversed.

Rejection of Claims 16-20 Under 35 U.S.C. §103(a) based on *Bois* in view of *Lai*.

To the extent that this ground for rejection relies on the reference *Bois*, the comments set forth above for claim 15 are incorporated by reference herein. Namely, that amended claim 15 includes limitations not shown in *Bois*, accordingly, all limitations are not shown by the cited reference and a prima facie case of obviousness has not been established.

In addition, with respect to claim 16, amended claim 16 includes the limitations of removing the stacked film pattern and subsequently forming a gate oxide film in a region between portions of the second oxide film.

Bois mentions MOS integrated circuits, but cannot be considered to enable the above

[9] See *Bois*, FIGS. 1-4, which show a single mask layer.

[10] See *Bois*, FIGS. 4 and 5, which shows a top surface of isolating dielectric 14 that appears to be coplanar with a bottom surface mask layer 4.

limitations of claim 16. *Lai* teaches away from claim 16, by forming a gate oxide layer prior to any isolation formation steps.[11]

Thus, the combination of references does not show or suggest all limitations of claim 16.

Claim 17 recites that a first electrode has end portions higher than a central portion. This limitation is not shown in the references.

The first reference *Bois* is silent as to electrodes, thus cannot show or suggest any particular arrangement of an electrode.

Lai shows a first polysilicon layer having ends, but such ends are not higher than a central portion of the layer.[12] *Lai* also shows a second polysilicon layer that is merged with the first polysilicon layer. However, no ends for such a layer are shown.[13] Thus, at best, *Lai* indicates it is possible to form ends for this second polysilicon layer at numerous locations. However, once again, this simply indicates the reference can be modified, not why such a modification would be pursued by one skilled in the art.

Accordingly, because claim 17 includes limitations not shown or suggested by the cited reference, this ground for rejection is traversed.

Amended claim 18 recites an insulating film top surface even with a top surface of the first electrode. These limitations are not shown in the cited combination of reference.

While the rejection is not clear about how specific claim elements correspond to features of the references, Applicant has assumed that the rejection is arguing that the isolating dielectric 14 of *Bois* corresponds to Applicant's "insulating film". Were *Bois* modified to incorporate the dual polysilicon layer structure of *Lai*, such an arrangement would result in a top surface of isolating dielectric being below any top surface of a gate electrode. [14]

Accordingly, the proposed combination of references, as best understood by Applicant, does not show all the limitations of amended claim 18.

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[11] See *Lai*, FIG. 2, which shows gate oxide 15 formed prior to thick field oxide regions 22.

[12] See *Lai*, FIG. 5, which shows first polysilicon layer 11 having end portions at the same level as a central portion.

[13] See *Lai*, FIG. 5, which shows second polysilicon layer 28. No end location is provided for such a layer, let alone an end position having the limitations cited in claim 17.

[14] See *Bois*, FIG. 5, which shows a top surface of isolating dielectric 14 that would appear to be even with a top surface of oxidized region 8, and hence below the top surface of any gate electrode formed subsequently.

The present claims 8-12 and 14-21 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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